Key Components of a PWB Material

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1. Organic resin
2. Inorganic filler
3. Copper conductor material

○ Requirements of an Insulator

The insulator selected should;

- Have high insulation resistance and breakdown voltage
- Have good mechanical strength
- Withstand corrosive chemicals used in processing
- Not absorb water
- Not degrade at process temperature
- Be also to drill through
- Not expand too much in the Z-direction
- Be able to dissipate heat in product use

- Base material, or the insulating board of a rigid PWB, is a sheet of laminate reinforced resin. - Epoxy, phenolic, and polyimide resin
- Reinforcing materials, or fillers are typically glass cloth, paper, asbestos, aramid, nylon
- Main parameters: Glass transition temperature, Tg, Hardness, brittleness, elastic modules, coefficient of thermal expansion(CTE), specific heat

Key properties of PWB base materials

Resin/Filler	T_g[℃]	Lateral CTE[ppm/℃]	ε (at 1 MHz)	Water absorption	Peel strength of foil [N/mm]
Phenolic/Paper	125	14 ... 18	4.5	0.75	>2.0
Epoxy/Glass(FR-4)	130	14 ... 18	4.9	0.15	>2.0
Polyimide/Glass	250	12 ... 16	4.5	0.35	>1.4
Polyimide/Quartz	280	6 ... 8	4.0	0.35	>1.2
Epoxy/Aramid	180	7 ... 9	3.9	0.44	>1.7
BT-Epoxy	185	13 ... 14	4.3	0.19	>2.0
Cyanate ester	240	-	3.7	0.40	>6.0
Polyimide/Aramid	230	7 ... 9	3.6	0.81	>1.6

○ Standard PWB materials

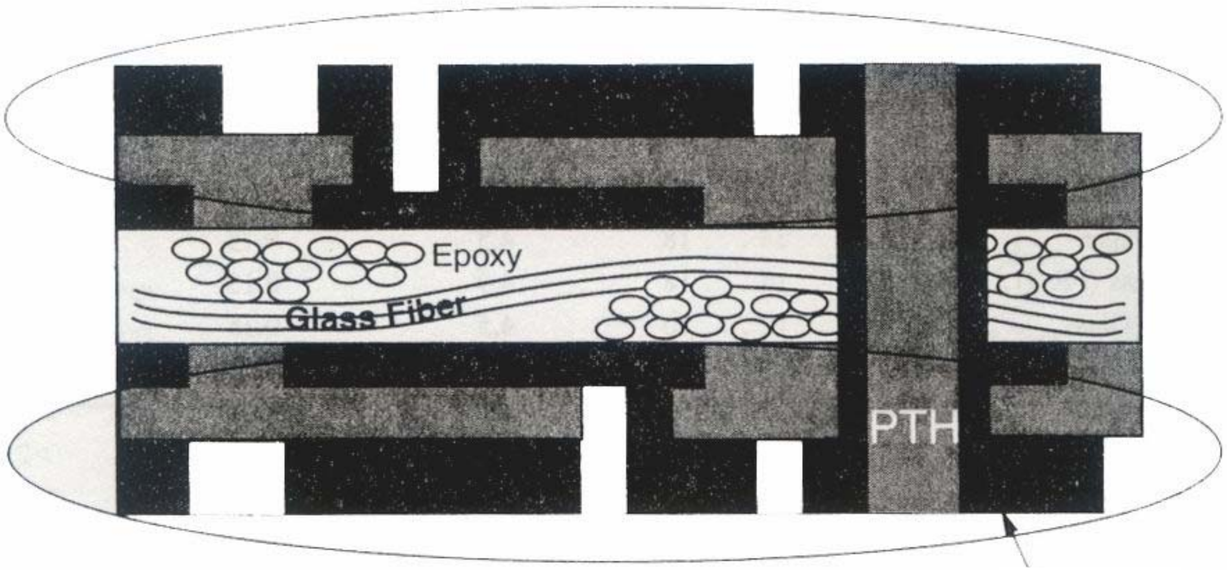
1. FR-4 epoxy-fiberglass laminate
   - Epoxy resin, Glass fiber, and Copper conductor

2. Resin-bromated

3. Polyimide-epoxy-resins are also used with fiberglass reinforcement for some special rigid PWBs required higher temperature for assembly → 350℃

○ Flexible PWB

Polyimide without reinforcement or with a low percentage of filler like quartz powder.
In some cases, photosensitive polyimide like dry films are used in order to make via formation easier and more economical.

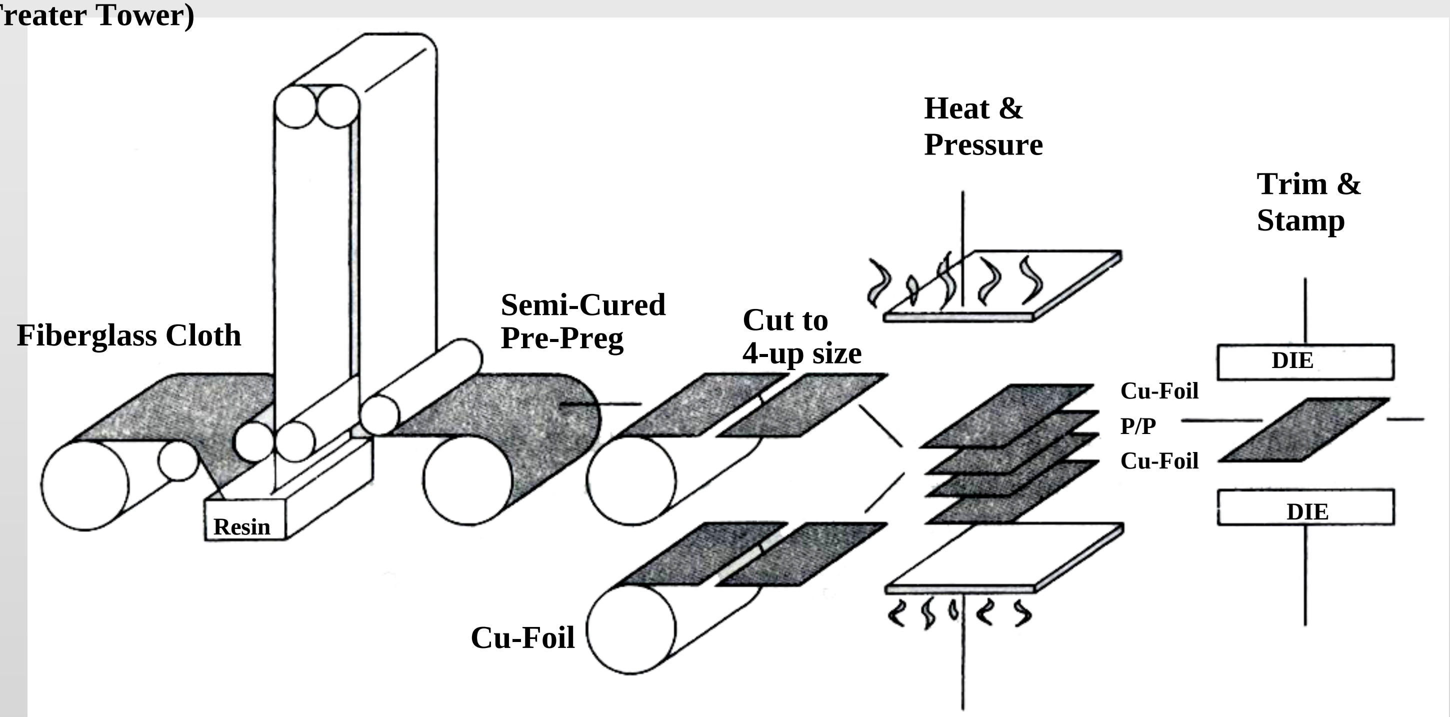


PTH : plated through hole

Copper

Elements of an FR-4 substrate

○ Production of Laminates



FR-4 grade laminate are:

1. Epoxy-resin suitably blended
2. Filler material in the form of glass cloth
3. Copper foil of required thickness : ~35μm(5μm for fine line)

Epoxy resin is a series of resin, which are derived from the reaction between bisphenol and epichlorohydrin, in the presence of a hardener.

The stages of laminate production are :

***Stage A* : Compounding. It is the activation of the epoxy-resin by mixing together precise amount of the resin components in a batch tank.**

***Stage B* : In order to impart mechanical rigidity to the final laminate, above resin blend is reinforced with glass fabric as filler material. As the filler material constitutes about 40-50% of the laminate bulkiness, it contributes significantly to mechanical, electrical and chemical properties of the laminate.**

***Stage C* : The C-staging operation is the final curing process after laminating the copper foil to the prepreg material.**

○ Advanced PWB Base Materials

FR-4 : Most widely used PWB material
- lowest cost, does not meet the high-performance requirements
- Dielectric constant, too high(4.9)
- Water absorption, too high
- CTE : ~17ppm/℃ ⇒ Si : 3ppm/℃
- T_g : 130℃ ⇒ SMT requirement : 220℃

Recent: thinner, smaller, faster interconnect, thermal resistance, ultra-thin dielectrics and small-hole formation
- These materials include high temperature resins such as BT epoxy, cyanate ester and polyimide.

Recent developments in PWB materials have been directed toward improving their **dimensional stability** and **surface smoothness**: **patterning of smaller feature,** reducing their **dielectric constant** and **dissipation factor** to meet the requirements for very high frequency RF application, and replacing glass reinforcement with laser processable materials to make **Laser drilling easier**.
-Linear lamination ⇒ glass filaments- instead of woven, very thin filaments

○ Aramid paper reinforced laminates, using paper-like nonwoven aramid fabric with epoxy-resin impregnation, exhibit very good dimensional stability with near-to silicon CTE, have a smooth surface and can be easily processed by Laser.

○ Advanced Resin System

Resin systems are moving toward higher T_g and better electrical properties than Conventional epoxy. The T_g of 180 [℃] is proving to be very cost-effective.

Typical Resin Properties

Resin System	ε[1MHz]	T_g [℃]	Relative cost
FR-4-epoxy	3.5-3.60	125-135	1
Polyfunctional FR-4	3.5-3.60	140-150	1-2
High Temperature one component epoxy system	3.90-4.00	170-180	3-6
Bismaleimide Triazine epoxy(BT)	3.2-3.30	180-190	3-6
Polyimide epoxy	3.5-3.6	250-260	10-20
Cyanate ester(CE)	2.80-3.50	240-250	20-30
Polyimide	3.30-3.40	>260	10-20
PTFE(melting point)	2.03-2.09	327	10-15

○ Advanced Filler System -Glass fiber: E-Glass, S-Glass, D-Glass

Composition	E-Glass	S-Glass	D-glass	Quartz	Kevlar	Technora HM-50
SiO_2	52-56	64-66	73-75	99.97		
Al_2O_3	12-16	22-24	0-1			
CaO	15-25	<0.01	0-2			
MgO	0-6	10-12	0-2			
B_2O_3	8-13	<0.01	18-21			
Fe_2O_3	-	0.1	-			
Zr_2O_3	-	<0.1	-			
CTE [10^{-6}/K]	5.01	2.80	2.00	0.54	-5.20	-7.50
ε(1MHz)	5.80	4.52	3.95	3.78	4.00	4.00
Thickness [mm]	0.05-0.23	0.06-0.18	0.06-0.18	0.08-0.13	0.1	0.1

Kevlar : Quartz and aramid

○ CTE of materials in the x-y direction : ppm/℃)

Materials	Substrate Type (x-y direction : ppm/℃)	PWB Type (z-direction: ppm/ ℃)
Epoxy/E-glass	13-17	75-95
BT Epoxy/E-glass	12-16	72-83
Polyimide/E-glass	12-15	67-76
CE/E-glass	11-14	52-62
Epoxy-Quartz	8-13	70-81
BT-Epoxy/Quartz	8-11	63-75
Polyimide/Quartz	8-11	61-71
CE/Quartz	8-9	50-60
Epoxy/Aramid	7-11	90-100
BT Epoxy/Aramid	6-10	82-92
Polyimide Thermount/Aramid	6-10	84-95
CE/S-glass	8.5-10	45-55
CE/S-glass(4HS)	7-9	45-55

BT : Bismaleimide Triazine

CE : Cyanate Ester

○ Standard PWB fabrication

PWB process flow :

CAD output technology files

↓

Prepare Mask

↓

Prepare copper clad laminate(cleaning, brushing)

↓

Apply photoresist on laminate

↓

Image (expose, develop) using mask

↓

Strip resist

↓

Sub-etch pattern

↓

(Repeat steps as necessary)

↓

Drill holes

↓

Through-hole plate for double side and multilayer boards

↓

Protect copper with Sn-Pb solder

↓

Solder mask/legend print

▷ Imaging

Feature size : < 200μm

1. **Clean surface**
2. **Apply photoresist**
3. **Expose photoresist**
4. **Develop photoresist image**
5. **Pattern transfer image (plating or etch)**
6. **Strip photoresist**

Photoresist materials are either liquids or dry films.

Liquid resists are used for precision work(Typically 50μm)

▷ Drilling

Drill smear is the most important factor determining hole quality.

Drill smear is caused by grinding the heat resin chip debris into the Hole wall.

Temperature :

Copper internal plane : ~ 150℃ in a functional land
~230℃ in a nonfunctional land

Woven drill : ~205℃ in a functional land
~650℃ in a nonfunctional land

▷ Platting

- High electrical conductivity
- Good mechanical strength
- High ductility and elongation
- Excellent solderability
- Good tarnish and corrosion resistance
- Good etchant resistance

▷ Electroplating is used to protect copper by plating Sn or SnPb, and by deposition of nickel as a solder barrier as an undercoat.

▷ **Etching**

-Resist stripping

-Precleaning

-Etching

-Neutralization

-Water rinsing

-Drying

*** Control parameters : agitation, temperature, pH, bath concentration**
regeneration of bath constituents

○ Limitations in standard PWB process

-Resist stripping
-Precleaning
-Etching
-Neutralization
-Water rinsing
-Drying

* Control parameters : agitation, temperature, pH, bath concentration
regeneration of bath constituents

1. New Products require Higher Pad Densities

-The pitch and area density of component connections ultimately drives PWB design and its processing technology.

-In general, increased lead or pad density of PWB is achievable through a trade off in substrate layer count, via size, and circuit line width and space.

-Above a threshold of approximately 20-30 pads/cm^2

-Leading portable equipment has pad densities in the range of 35-90 pads/cm^2.

-The higher pad density is achieved by so-called microvia technology.

2. Drilled-Hole Technology Becomes Too Expensive

- Drilled holes and vias are among the basic structures of PWBs; However, they have two main problems:

1) They take up too much space on the board and do not provide high pad densities.
2) They become expensive as their size is lowered.
Standard drill technology can produce a via pad size of 0.025-in with a 0.014- to 0.015-in drilled hole. But as the hole size decreases, they get very expensive, wherein the cost of drilling has gone up by a factor of 18 times.
As a result, small-hole drilling alone can contribute as much as 30-40% of the total cost of the PWB.
Also, as the holes get smaller for the same board thickness, aspect ratio increases. This tends to decrease reliability as high-aspect holes have problems in getting sufficient plating solution and solder into the hole.

3. Microvia Solves these Two Problems

▷ Microvia, or Blind via, in form of non-drilled blind and buried vias.

1) Laser drilling
2) Plasma or reactive ion etching
3) Photolithography

▷ PWBs with microvias offer the following advantages for high-volume production:

- Increased circuit density
- Advanced package enable
- Better electrical performance
- Improved reliability in comparison with drilled through-holes
- Improved thermal conduction through the thin dielectric films
- Lower PWB cost

4. Methods of Microvia Generation

▷ **Photovia process**

The low-cost photovia processing requires layers of photoimageable or photosensitive permanent dielectric materials. They are exposed through a mask to form the via and windows of any geometry defined by the mask. The exposed and developed films are then cured to obtain the final cross-link properties of that polymer.

▷ **Plasmavia process**

Plasma-etched via(PEV) technology applies vacuum processing to remove the polyimide dielectric layer.
Typical via holes are 60-90μm in diameter.

▷ **Laservia process**

CO2, UV excimer laser, UV Nd:YAG

▷ **Paste-Via Process**

After the holes are opened into a single dielectric layer, they are filled with conductive paste.

▷ **Photovia technology is very productive, resolution is high, but provide irregular hole wall quality, and needs special photodielectric materials**

▷ **Plasmavia process provides even hole uniformity and cleanliness, is productive, but needs expensive equipment**

▷ **Laservia drilling provides very clean surface and suitable wall shape, is very flexible, but less economic than photovia processing**

▷ **Paste-Vias are very cheap, but less reliable than wall metallized vias**

○ **Microvia Boards**

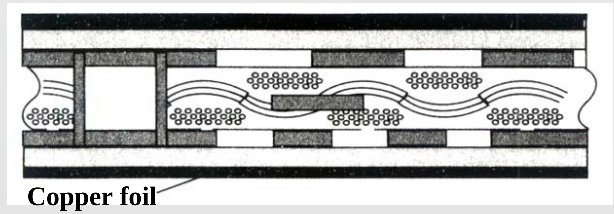
▷ **Microvia boards are fabricated by three major technologies:**

1. **Surface Laminar Circuitry(SLC) or build-up technology**
2. **All Layer Internal Via Hole(ALIVH) technology**
3. **Buried Bump Interconnection Technology(B^2IT)**

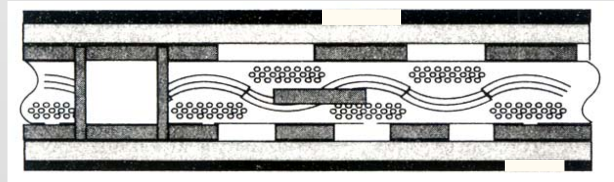
1. Build-up Technology

▷ Sequential build-up(SBU) technology using photovias

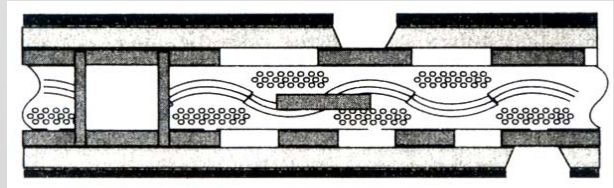
Production of Mass-Laminate



Copper Etching



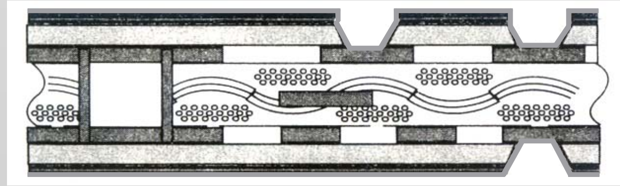
Laservia formation CO_2 Laser



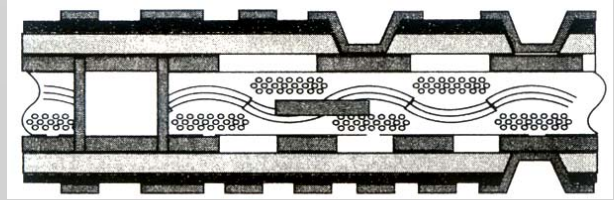
Desmear treatment Catalyzing

Surface is little more roughened by desmear treatment

Electroless copper plating



Patterning by Etching and Electrolytic plating



○ **The key to build-up technology**

- Via formation, which is achieved either with photosensitive polymer technology or with laser technology.
- In photopolymer technology, photosensitive epoxy, polyimide, benzo-cyclobutene or other photopolymer dielectric materials (typical thickness after coqating and curing : 20-40μm) are used.
- Via diameter : 50-100μm

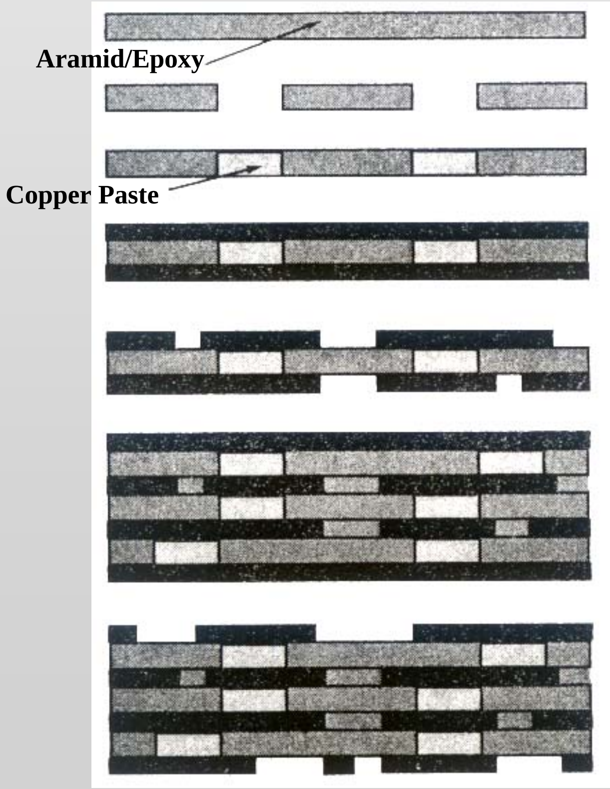
▷ **In laser process technology, the dielectric used is non-photosensitive**

▷ **Copper lines and spaces are patterned as small as 20μm wide.**

2. All Layer Internal Via Hole (ALIVH) Process

▷ **This process is very similar to the ceramic substrate process, except for the fact that the greensheet in the ceramic process is replaced with a permanent organic dry film.**
The different layers, each containing insulating and conducting layers, are fabricated separately, and then they are unified a single lamination process.

ALIVH Technology



(All Layer Internal Via Hole)

3. Bumped Buried Interconnection (B^2IT) Technology

▷ This process involves the use of silver bump paste metallization to pierce holes through the dielectric or prepreg, thus providing microvia interconnections.

B^2IT Technology